

## TIPS and Hints on PCB Layout

I have been asked often about tips for good layout practice and how it relates to PC Board manufacturability. After 22 years in the business of layout, filmtooling and exposure to circuit board manufacturing, I have accumulated a vast working knowledge of this industry. I have compiled some of my knowledge and opinions in this document. The hour or two it takes to understand these concepts will pay for itself again and again.

Fundamentally: your circuit board layout data is directly used to combine several different manufacturing processes for the creation of your printed circuit boards. Your basic 1-UP board data is the foundation that all the mechanical, photographic, plating, etching, silkscreen, and test tooling is created from during the manufacture of your board. The correctness of this data directly relates to the final product produced. Your board pricing is partially determined by base cost, turnaround time "but" also by the expected yield and ease of production.

To get the finished circuit board to represent your design, the data must be modified and made manufacturable. (Design For Manufacturing-DFM) then your data will be CAMEd up in panel form (CAM-Computer Aided Manufacturing)

Only specialty houses produce one board at a time. Your data will be used as the basis of a panel of circuit boards. At the board house "DFM" and "CAM" will be performed on your one up board image then the results will be arrayed into the panel. Do not attempt to array, this just multiplies the work to prepare the data for the panel.

## PCB Data Files

You should understand the data you expect someone to use to create your circuit boards from. All data that you will send to a board house is in "ASCII" meaning you can read this data with any text editor. (If it looks Egyptian it's not ASCII)

You will generally only need to send out two flavors (file types) of ASCII data. One is Numerical Data (NC) for drill and or route files (identified by having tool codes (T-CODES) and vector coordinates X\*\*\*\*Y\*\*\*\*\* for positions.

The second is Gerber data for film tooling (identified by a format statement with add= aperture d-code definitions and d-codes or shape / draft codes prior to vector coordinate strings). Aperture tables are no longer required if you have a relatively newer layout package. The Gerber data is usually written in Gerber extended (RS274X) or in fire9000.

If your software is still generating Gerber (RS274D) then you will need to create and send a single "Unified" aperture table file. You can tell that your sending RS274D by looking at the beginning of the file and not seeing any aperture D-CODE definition (%ADD) statements. (Map files are not aperture tables) an aperture table file should list sequentially all the used D-CODES for the entire job usually starting at D10 which includes the shape and size. (It helps if you note some where what layout software and version name generated this aperture file so that software can be used to associate the apertures with the Gerber data).

\*\* All too often I receive 25 files for a board design when only five of these files will ever be used. This is the lazy mans way of generating data for a circuit board house!! There are over fifty different layout software's generating files with every possible file name and extension, or acronym. Each file must be examined to determine if this file is something we need or need to dispose of. I have seen assembly drawings used as silk screens and solder masks that covered over surface mount pads because there were three or four files that looked almost the same and the wrong file was chosen. Again understand your data and send only the data files that are needed to create the board. There are several inexpensive Gerber data viewers available. (Usually costing less than \$500 -this is less than the cost of one bad board build)  
I cannot tell you how many times I have heard "well that is not what it looked like in my layout software". Your layout software does a conversion process to generate the Gerber data and this conversion is not always true or WYSIWYG! (What You See Is What You Get).

I get asked about what format the data should be output in. Generally- Gerber data should be 2.4 leading zero suppression, absolute.

N/C data should be 2.4 trailing zero suppression.

What is the format 2.4 verses 5.3? This refers to the number of inch and decimal digits. since we can assume no circuit board is over 99 inches the first digit should never need to be larger than two, the second number is accuracy 3 is sufficient in most cases but 4 is better and most software can only recognize up to 6 decimal digit places.

What and why, ZERO SUPPRESSION-numerical machines do not recognize decimals so this is really telling a machine to either read the data number from left to right or right to left and to drop the decimal point and remove irrelevant or unused zeros.

Absolute verses incremental - data coordinates written that are relative to a datum "zero" is "absolute data." data written "relative to the last known coordinate" is "incremental". (Incremental data can accumulate decimal rounding errors and should not be used).

An additional hint; When you use true poly boundaries (found in some types of power and ground planes and or true-type text styles), The software can make rounding errors when outputting 2.4 format. Your layout software may have 2.6 or greater native resolution. This reduction can cause major invalid polygon problems. To help resolve this issue, set your output at the highest resolution possible up to 6 places. There are lots of rules about polygons, the first rule is that a polygon cannot have more than fifty thousand sides and it cannot crossover itself. (A single line bowtie is an invalid polygon)

## Board Layouts

Always create a label to identify each data layer.

Always create your data at 1/1 (the days of reductions are over)

No dimensions or reduction bars are needed (the days of reductions are over) if you have a good boundary (board edge) definition.

Targets - good practice but only if they occur on all layers and are moved away from board data by at least 1/2 inch- these are used as a quick reference to check for data line up then they are discarded.

Flipping of layers- do not mirror or flip layers, data is assumed right reading thru the board component side to solder side (all layers should be in register.)

(Tip if your software is not generating files in register then try the following:  
Draw a box around the entire board. Make the box 1-inch larger than entire data set and on all layers. Now you can generate the output.)

Layout on a Grid;

Standard inch grids are: .100, .050, .025, .010, .005, .001

Standard metric grids are: 1mm .5mm .25mm .01mm

Fractions are used by carpenters

Use logical board layout conventions. What does this mean?

Simple layout guidelines are.

Pads-pads should be at least .020 over finished drill size for 1-ounce copper boards and preferably at least twice the diameter of the drill for components. Octagons, diamonds, round cornered rectangles, and smiley faces are not pads but are flashed shapes. Pad shapes are round, square, oblong or oval, rectangle, and thermal. No pad may be larger than 1 inch in size. (A custom pad shape cannot have more than one hundred vertices)

Try to keep definition between pads and traces.

(Why? in QC it is much easier to spot missing or plugged holes in pads rather than along or at the end of a trace)

Traces-traces should always terminate to the center of a pad.

Tie points- 4 way crosses should be avoided, stagger these connections. (First it makes for 4 right angle acid traps and second it looks like a routing error and raises a red flag and asks for a phone call to just check).

Traces sizes; use largest allowable but try to be consistent! For good plating and improved yield 3- .020 mil traces side by side will plate/etch better than a .010, .030, and a .010. The potential to damage a .010 is much greater than that of a .020. For every .005 below .020 trace width you can expect reduced yields by 5% just due to normal handling and imaging issues. Most traces are drawn with a round but can be square on the x and y-axis only and can never be over 1 inch in size.

Trace width –what do I use? Simply put- trace spacing has everything to do with voltage (arc and leakage). Trace width and copper weight has everything to do with current! (If you want to know what trace width to use for what current there are dozens of tables on the internet and I have several but to understand how to use the tables has more to do with you knowing about allowable thermal rise verses trace width and weight).

Simply -at what point do you create a fuse, resistor or momentary light-bulb rather than a conductor? How much heat can you generate before it becomes a problem - passing current along a conductor means heat- know your circuits ability to generate and dissipate heat along a conductor.)(Never encapsulate something that generates heat).

Laying out in a logical fashion without acid traps.

Traces should be on grid and laid horizontal, vertical or at 45 degrees. No traces should form a less than 90-degree angle. all right angles should be filleted with a 45-degree (why? all boards are acid etched and acid pools in the corners of any angle, the smaller angle the more acid dwell time causing uneven etching and even possibly etch undercutting).

Auto-routing -the design will only be as good as the rules you are able to define for your autoroute software to use. In autoroute software you get what you pay for. The results directly affect the buildability of the PC Board. Most "good designers" only use the autoroute results to generalize the layout and then hand adjusts the layout. (typical auto-route routines run traces or groups of traces along the shortest path to a given area using the minimum clearance rules to get there. this causes "the layout to have minimum trace and space issues all across the design". the autorouters usually ignore all the free space available to route in. by freeing up the layout manually using that free space you make your board much more buildable and therefore increase your yield and reduce your price.

Holes-

Plated-drill sizes should be at least .005 larger than the max tolerance of the component lead diameter.

(why? because to plate the holes requires that the hole be drilled larger. ? how much on a 1-ounce board that oversize is .005 this gives you >1.5 mil copper wall x 2 sides is .003-.004 and standard hole tolerances are +/- .003. your drill sizes reflect finished drill diameter +/- .003)

Non-plated holes should be represented by a donut or a cross. do not use a pad of the same size as the diameter (you may or may-not end up with a plated hole) you should allow +/- .005-7 for positional tolerance of this hole as non-plated holes are either a second drill operation or a rubber plugged plating operation. Slots are routed, not drilled, avoid if you can.

Add .003- .005 to all layout features for each additional ounce copper over 2-ounce this will allow for normal etch loss.

plating and photoprocessing-you should be aware that the photo-process used in the standard board manufacturing process always loses .002 on all feature widths and should be considered when laying out fine pitched circuit boards. (what? two scenarios if nothing is changed during DFM and cam- 1. a board layout with 6 mil traces / spaces will yield you a board that has 4 mil traces and 8 mil spaces between conductors. 2. a board with 15 mil pads and 10 mil holes will yield a 13 mil pad with questionable plating in the hole due to etch migrating into the hole).

Board profile vs. corner marks and how big? The new software used by board houses can program the routing routine from your board profile. I like at least one layer preferably the mask layer having a complete board profile of a .008- .010 in width to create the route routine.

(after creating the route n/c file, I will normally change this profile to .050 x .050 x .010 corner marks on the mask layers and remove all other board profile references -except on reverse plane layers which should be .030- .040 wide for copper relief from the board edge.

Hot air level verses tin-lead plate - first the hot air level process is dipping a fluxed board or board panel in a molten bath of tinlead and then using airknives excess solder is blown thru the holes and off the panel.

Tin lead plate is a globally plated process that is brightened in a vat of oil heated to the melting temperature of the tinlead where the tin floats to the top. Hot air leveled boards have a fraction of the lead than a tin lead plated board. Lead is becoming a long term environmental disposal issue. During the assembly of a plated board the solder wave flow or reflow will cause the lead to go molten under solder mask causing wrinkling of the mask.

It is in the board houses interest to minimize the amount of waste treating of lead laden liquids.

Solder mask and size - it used to be that solder mask was a silkscreened pattern applied to a PC Board and you had to allow for screen stretch during the run and miss-alignment. No longer is it being done that way, it is a photographic process using the film image in position to harden or crosslink the mask across a flood coated panel. Today most board houses use a liquid photo-imagable solder mask. (LPI mask) registration is usually within .003. Screenable soldermask pads were usually between .010 and .020 larger than the conduction pads. A general rule today is to make them .006- .008 over the pad size and .004 on tight boards.

Soldermask verses no soldermask? Solder mask is a low or non-permeable coating that serves several functions. The first is to protect all non-solderable conductors against corrosion. The mask seals the board base material against the absorption of moisture, and fluxes "a corrosive". Lastly it assists in assembly by creating a dam between solderable conductors during reflow. During reflow the molten solders surface tension wants to draw solder to itself and not across something that is dissimilar.

Solder mask over vias or feed thru's - via's can be used as test points if they are not covered by mask. If you wish to cover via's with mask at least one side should have a vent of one half the diameter of the via hole to allow entrapped gas and moisture to escape and not bubble during thermal cure.

Silkscreen legend-parts legends are still a silkscreened pattern applied to the PC Board except in the largest production houses, which use a liquid photo-imagable process, or an ink jet process.

To obtain opacity and prevent the drying in of the ink (usually white) requires that the legend features be of a .008 or larger aperture. Epoxy ink is screened thru a course mesh containing an applied open legend image in a photographic capillary emulsion.

Stair stepping of straight lines due to legend and coincidently screen frequency becomes less noticeable at a .010 or larger feature sizes.

Clearing of silkscreen legend over drilled holes - clearing of silkscreen data may be done due to silkscreen ink inhibiting solder reflow during assembly. Silkscreen legend ink should fit the mask image and not extend onto solderable surfaces of a PCB. Silkscreen legend may cover via holes and pads if all vias are covered with mask or if the vias are of a unique size so that these can be excluded from the clear silkscreen process.

Tear dropping or snowmanning of pads may be done on request. Teardropping strengthens the junctions between pads and traces.

Teardropping is vectors from one trace diameter filleting to the pad,

Snowmanning is a pad half the diameter of the pad that has a trace intersecting; this pads origin is placed automatically at the pad edge. The current software's limitation for teardropping or snowmanning is limited to traces terminating at flashed round, square and rectangular pads. (Ovals, polygons and special shapes do not automatically tear drop and would have to be done manually)

Solder paste- the data is usually of the same size as the pads on the board. This allows the assembly house to specify the reduction percentage that the stencil manufacturer will use to create the paste stencil. (the type of paste and the method their screening machine uses determines the reduction percentage. solder paste files can be generated to fit the panel data the board house creates if you are buying circuit board panels scored or paper doll routed. just let the board house know that you will require this data.

Fiducials- used for automated assembly. Generally fiducials are 1mm (.03937") round on the copper outer layers and 2mm (.07875") round on the mask layers (usually rounded to 40 and 80). They may also be diamonds, squares, or octagons. (Ask your assembly house for their preference). Usually only two are required per board and four on panels with rails.

Fabrication drawings- what a bonus if you generate one. It is the specification that the board house must live by. all data supplied is in a numerical format, therefore minimal dimensioning is required, (usually just a couple of overalls) but base material, layer stack-up sequence, finished copper weight, solderable finish, solder mask color and gloss, silkscreen color, flatness, annularity and tolerances are supplied here. If you need a sample list of what should be contained just ask.

#### DRC- Design Rule Checking

I have seen several circuit board houses tout that they run a DRC on all board designs.

What does this mean? Not much! What Design Rule Check are they running? What rules? Is it a set of rules that yields good boards "most" of the time, or all of the time?

What about boards that are not laid out in a logical fashion, do they just ignore these violations (probably), fix them (if there is time), or turn back the job (not in today's market). I can set all the rules to .004 pad to pad, trace to trace and pad to hole and trace to pad and get everything to run without any violations on a logical board layout.

Depending on these rules you can still end up with bad circuit boards. Circuit boards that tested well but cannot be assembled without problems. I can also run the same DRC and end up with literally hundreds of violations on a non-logical board layout. (If you want a DRC run then you must have a logical board layout, and defined design rules that apply to your particular board and board application).

Examples: the design rules would be much different for each of these type PC Boards. a landscape critical low voltage high-speed digital busboard utilizing controlled impedance with 6 mil traces and spaces and .010 mil vias.

What about the design rules for a feature critical strip line microwave antenna?

Now consider the DRC for a 4 ounce power supply amplifier board with lots of current and heat with isolated locations generating greater than a thousand volts, this single board needs two different sets of design rules.

(Are PC Board houses equipped with engineers for cam operators and given the application specifics that would establish the type of design rules necessary for a board of this type?)

Last but not least:

INSTANT CIRCUIT BOARDS-- the Xerox machine that takes your layout data in one side and spits out perfect printed circuit boards on the other side cannot be used on your job.

One of the following applies

1. Your material spec calls for something other than INVISIUM.
2. Your plating spec calls for something other than UNOBTAINIUM.
3. Your P.O. total is different from the total in the UCAN'TAFFORDIUM total box.

If you can change you material to INVISIUM then your boards are ready and sitting on the corner of your desk. If you can find some UNOBTAINIUM then we can get our machine working again. If you can change the total in the UCAN'TAFFORDIUM total box to a sum greater than \$2,000,000 then when the check clears we'll deliver the boards and split the balance.